

AMENDMENTS TO THE CLAIMS

1 1. (Currently Amended) A method of generating a communication frequency
2 based on a modulo 23 solution for an input variable, comprising:
3 receiving an input variable;
4 generating an intermediate modulo 23 solution by:
5 generating a binary representation of said input variable;
6 using the five rightmost digits of said binary representation of said input variable
7 to represent a first intermediate remainder (R');
8 using the remaining three leftmost digits to represent a first intermediate quotient
9 (Q');
10 expressing said first intermediate modulo solution as a sum of said first
11 intermediate quotient (Q') multiplied by 9 plus said first intermediate
12 remainder (R'); and
13 comparing said first intermediate modulo solution to the quantity 32;
14 indicating said first intermediate ~~remainder (R')~~ modulo solution as the modulo
15 remainder (R) if said quantity of said first intermediate modulo solution is less
16 than ~~32~~ 23; and
17 using said modulo remainder to generate said communication frequency.

1 2. (Currently Amended) The method according to claim 1 wherein an iterative
2 process is performed if said first intermediate modulo solution is greater than 32, said iterative
3 process comprising:
4 (a) generating a binary representation of said first intermediate modulo solution;
5 (b) using the five rightmost digits of said binary representation of said first
6 intermediate modulo solution to represent a second intermediate remainder (R'')
7 (c) using said remaining three leftmost digits to represent a second intermediate
8 quotient (Q'');

- (d) expressing said second intermediate modulo solution as a sum of said second intermediate quotient (Q'') multiplied by 9 plus said second intermediate remainder (R'');
- (e) comparing said second intermediate modulo solution to the quantity 32;
- (f) indicating said second intermediate ~~remainder (R'') modulo solution~~ as the modulo remainder (R) if said quantity of said second intermediate modulo solution is less than ~~32~~ 23; and
- (g) repeating steps (a) through (f) if said intermediate modulo solution is greater than 32 ~~and continuing until the intermediate modulo solution is less than 32.~~

3. (Original) The method according to claim 1, wherein said multiplication of said first intermediate quotient (Q') by 9 is accomplished by:

shifting said binary representation of Q' to the left by three places; and

adding said left-shifted value of Q' to the original value of Q' .

4. (Original) The method according to claim 2, wherein said multiplication of said second intermediate quotient (Q'') by 9 is accomplished by:

shifting said binary representation of Q'' to the left by three places; and

adding said left-shifted value of Q'' to the original value of Q'' .

5. (Currently Amended) A method of generating a modulo 79 solution for an input variable, comprising:

receiving an input variable;

generating an intermediate modulo 79 solution by:

generating a binary representation of said input variable;

using the seven rightmost digits of said binary representation of said input variable to represent a first intermediate remainder (R');

using the remaining leftmost digits to represent a first intermediate quotient (Q');

expressing said first intermediate modulo solution as a sum of said first intermediate quotient (Q') multiplied by 49 plus said first intermediate remainder (R'); and
comparing said first intermediate modulo solution to the quantity 128;
indicating said first intermediate ~~remainder (R')~~ modulo solution as the modulo remainder (R) if said quantity of said first intermediate modulo solution is less than ~~128~~ 79; and
using said modulo remainder to generate said communication frequency.

6. (Currently Amended) The method according to claim 5 wherein an iterative process is performed if said first intermediate modulo solution is greater than 128, said iterative process comprising:

- (a) generating a binary representation of said first intermediate modulo solution;
- (b) using the seven rightmost digits of said binary representation of said first intermediate modulo solution to represent a second intermediate remainder (R'');
- (c) using said remaining leftmost digits to represent a second intermediate quotient (Q'');
- (d) expressing said second intermediate modulo solution as a sum of said second intermediate quotient (Q'') multiplied by 49 plus said second intermediate remainder (R'');
- (e) comparing said second intermediate modulo solution to the quantity 128;
- (f) indicating said second intermediate ~~remainder (R'')~~ modulo solution as the modulo remainder (R) if said quantity of said second intermediate modulo solution is less than ~~128~~ 79; and
- (g) repeating steps (a) through (f) if said intermediate modulo solution is greater than 128 ~~and continuing until the intermediate modulo solution is less than 128.~~

7. (Original) The method according to claim 5, wherein said multiplication of said first intermediate quotient (Q') by 49 is accomplished by:
shifting said binary representation of Q' to the left by 5 places to define a first shifted Q' value,

shifting said binary representation of Q' to the left by 4 places to define a second shifted Q' value; and
adding said first and second shifted values of Q' to the original value of Q' .

8. (Currently Amended) The method according to claim 6, wherein said multiplication of said second intermediate quotient (Q'') by $4Q$ is accomplished by:
shifting said binary representation of $[[Q']][Q'']$ to the left by 5 places to define a first shifted $[[Q']][Q'']$ value,
shifting said binary representation of $[[Q']][Q'']$ to the left by 4 places to define a second shifted $[[Q']][Q'']$ value; and
adding said first and second shifted values of $[[Q']][Q'']$ to the original value of $[[Q']][Q'']$.

9. (Currently Amended) A system for generating a communication signal at a predetermined frequency, comprising:
a transceiver, said transceiver comprising:
a radio frequency module;
a baseband core further comprising a frequency control functionality;
a frequency hopper within said baseband core of said transceiver, said frequency hopper being operable to generate a plurality of frequencies related to a modulo 23 solution of an input variable, wherein said frequency hopper generates an intermediate modulo 23 solution by:
generating a binary representation of said input variable;
using the five rightmost digits of said binary representation of said input variable to represent a first intermediate remainder (R');
using the remaining three leftmost digits to represent a first intermediate quotient (Q');
expressing said first intermediate modulo solution as a sum of said first intermediate quotient (Q') multiplied by 9 plus said first intermediate remainder (R');
comparing said first intermediate modulo solution to the quantity 32; and

indicating said first intermediate ~~remainder (R')~~ modulo solution as the modulo remainder (R) if said quantity of said first intermediate modulo solution is less than ~~32~~ 23.

10. (Currently Amended) The ~~method~~ system according to claim 9 wherein an iterative process is performed if said first intermediate modulo solution is greater than 32, said iterative process comprising:

- (a) generating a binary representation of said first intermediate modulo solution;
- (b) using the five rightmost digits of said binary representation of said first intermediate modulo solution to represent a second intermediate remainder (R'');
- (c) using said remaining three leftmost digits to represent a second intermediate quotient (Q'');
- (d) expressing said second intermediate modulo solution as a sum of said second intermediate quotient (Q'') multiplied by 9 plus said second intermediate remainder (R'');
- (e) comparing said second intermediate modulo solution to the quantity 32;
- (f) indicating said second intermediate ~~remainder (R'')~~ modulo solution as the modulo remainder (R) if said quantity of said second intermediate modulo solution is less than ~~32~~ 23; and
- (g) repeating steps (a) through (f) if said intermediate modulo solution is greater than 32 ~~and continuing until the intermediate modulo solution is less than 32~~.

11. (Currently Amended) The ~~method~~ system according to claim 9, wherein said multiplication of said first intermediate quotient (Q') by 9 is accomplished by: shifting said binary representation of Q' to the left by three places; and adding said left-shifted value of Q' to the original value of Q'.

12. (Currently Amended) The ~~method~~ system according to claim 10, wherein said multiplication of said second intermediate quotient (Q'') by 9 is accomplished by: shifting said binary representation of Q'' to the left by three places; and

4 adding said left-shifted value of Q'' to the original value of Q'' .

1 13. (Currently Amended) A system for generating a communication signal at a
2 predetermined frequency, comprising:
3 a transceiver, said transceiver comprising:
4 a radio frequency module;
5 a baseband core further comprising a frequency control functionality;
6 a frequency hopper within said baseband core of said transceiver, said frequency hopper
7 being operable to generate a plurality of frequencies related to a modulo 79
8 solution of an input variable, wherein said frequency hopper generates an
9 intermediate modulo 79 solution by:
10 generating a binary representation of said input variable;
11 using the seven rightmost digits of said binary representation of said input
12 variable to represent a first intermediate remainder (R');
13 using the remaining leftmost digits to represent a first intermediate quotient (Q');
14 expressing said first intermediate modulo solution as a sum of said first
15 intermediate quotient (Q') multiplied by 49 plus said first intermediate
16 remainder (R');
17 comparing said first intermediate modulo solution to the quantity 128; and
18 indicating said first intermediate ~~remainder (R')~~ modulo solution as the modulo
19 remainder (R) if said quantity of said first intermediate modulo solution
20 is less than ~~128~~ 79.

1 14. (Currently Amended) The ~~method system~~ according to claim 13 wherein an
2 iterative process is performed if said first intermediate modulo solution is greater than 128, said
3 iterative process comprising:
4 (a) generating a binary representation of said first intermediate modulo solution;
5 (b) using the seven rightmost digits of said binary representation of said first
6 intermediate modulo solution to represent a second intermediate remainder (R'')
7 (c) using said remaining leftmost digits to represent a second intermediate quotient
8 (Q'');

- (d) expressing said second intermediate modulo solution as a sum of said second intermediate quotient (Q'') multiplied by 49 plus said second intermediate remainder (R'');
- (e) comparing said second intermediate modulo solution to the quantity 128;
- (f) indicating said second intermediate ~~remainder (R'') modulo solution~~ as the modulo remainder (R) if said quantity of said second intermediate modulo solution is less than ~~128~~ 79; and
- (g) repeating steps (a) through (f) if said intermediate modulo solution is greater than 128 ~~and continuing until the intermediate modulo solution is less than 128.~~

15. (Currently Amended) The ~~method~~ system according to claim 13, wherein said multiplication of said first intermediate quotient (Q') by 49 is accomplished by:

shifting said binary representation of Q' to the left by 5 places to define a first shifted Q' value,

shifting said binary representation of Q' to the left by 4 places to define a second shifted Q' value; and

adding said first and second shifted values of Q' to the original value of Q' .

16. (Currently Amended) The ~~method~~ system according to claim 14, wherein said multiplication of said second intermediate quotient (Q'') by 9 is accomplished by:

shifting said binary representation of Q'' to the left by 5 places to define a first shifted Q'' value,

shifting said binary representation of Q'' to the left by 4 places to define a second shifted Q'' value; and

adding said first and second shifted values of Q'' to the original value of Q'' .

17. (Currently Amended) A system for generating communication frequencies in a wireless interface system that services communications between a wirelessly enabled host and at least one user input device, comprising:

a wireless interface unit that wirelessly interfaces with the wirelessly enabled host,
wherein the wireless interface unit comprises:
an analog module including a transceiver unit and a frequency synthesizer,
a baseband module including a frequency hopper, wherein said frequency
hopper is operable to generate a plurality of frequencies related to a
modulo 23 solution of an input variable, wherein said frequency hopper
generates an intermediate modulo 23 solution by:
generating a binary representation of said input variable;
using the five rightmost digits of said binary representation of said input
variable to represent a first intermediate remainder (R');
using the remaining three leftmost digits to represent a first intermediate
quotient (Q');
expressing said first intermediate modulo solution as a sum of said first
intermediate quotient (Q') multiplied by 9 plus said first
intermediate remainder (R');
comparing said first intermediate modulo solution to the quantity 32; and
indicating said first intermediate remainder (R') modulo solution as the
modulo remainder (R) if said quantity of said first intermediate
modulo solution is less than ~~32~~ 23; and
wherein said frequency synthesizer is operable to generate a frequency
hop sequence using said result of said modulo 23 solution
generated by said frequency hopper.

18. (Currently Amended) The system according to claim 17 wherein an iterative
process is performed if said first intermediate modulo solution is greater than 32, said iterative
process comprising:

- (a) generating a binary representation of said first intermediate modulo solution;
- (b) using the five rightmost digits of said binary representation of said first
intermediate modulo solution to represent a second intermediate remainder (R'')
- (c) using said remaining three leftmost digits to represent a second intermediate
quotient (Q'');

- (d) expressing said second intermediate modulo solution as a sum of said second intermediate quotient (Q'') multiplied by 9 plus said second intermediate remainder (R'');
- (e) comparing said second intermediate modulo solution to the quantity 32;
- (f) indicating said second intermediate ~~remainder (R')~~ modulo solution as the modulo remainder (R) if said quantity of said second intermediate modulo solution is less than ~~32~~ 23; and
- (g) repeating steps (a) through (f) if said intermediate modulo solution is greater than 32 ~~and continuing until the intermediate modulo solution is less than 32.~~

19. (Currently Amended) The ~~method~~ system according to claim 17, wherein said multiplication of said first intermediate quotient (Q') by 9 is accomplished by:
shifting said binary representation of Q' to the left by three places; and
adding said left-shifted value of Q' to the original value of Q'.

20. (Currently Amended) The ~~method~~ system according to claim 18, wherein said multiplication of said second intermediate quotient (Q'') by 9 is accomplished by:
shifting said binary representation of Q'' to the left by three places; and
adding said left-shifted value of Q'' to the original value of Q''.

21. (Currently Amended) A system for generating communication frequencies in a wireless interface system that services communications between a wirelessly enabled host and at least one user input device, comprising:
a wireless interface unit that wirelessly interfaces with the wirelessly enabled host, wherein the wireless interface unit comprises:
an analog module including a transceiver unit and a frequency synthesizer,
a baseband module including a frequency hopper, wherein said frequency hopper is operable to generate a plurality of frequencies related to a modulo 79 solution of an input variable, wherein said frequency hopper generates an intermediate modulo 79 solution by:

generating a binary representation of said input variable;
 using the seven rightmost digits of said binary representation of said input variable to represent a first intermediate remainder (R');
 using the remaining leftmost digits to represent a first intermediate quotient (Q');
 expressing said first intermediate modulo solution as a sum of said first intermediate quotient (Q') multiplied by 49 plus said first intermediate remainder (R');
 comparing said first intermediate modulo solution to the quantity 128; and
 indicating said first intermediate ~~remainder (R')~~ modulo solution as the modulo remainder (R) if said quantity of said first intermediate modulo solution is less than ~~128~~ 79.

22. (Currently Amended) The system according to claim 21 wherein an iterative process is performed if said first intermediate modulo solution is greater than 128, said iterative process comprising:

- (a) generating a binary representation of said first intermediate modulo solution;
- (b) using the seven rightmost digits of said binary representation of said first intermediate modulo solution to represent a second intermediate remainder (R'');
- (c) using said remaining leftmost digits to represent a second intermediate quotient (Q'');
- (d) expressing said second intermediate modulo solution as a sum of said second intermediate quotient (Q'') multiplied by 49 plus said second intermediate remainder (R'');
- (e) comparing said second intermediate modulo solution to the quantity 128;
- (f) indicating said second intermediate ~~remainder (R'')~~ modulo solution as the modulo remainder (R) if said quantity of said second intermediate modulo solution is less than ~~128~~ 79; and
- (g) repeating steps (a) through (f) if said intermediate modulo solution is greater than 128 ~~and continuing until the intermediate modulo solution is less than 128.~~

1 23. (Original) The system according to claim 22, wherein said multiplication of
2 said first intermediate quotient (Q') by 49 is accomplished by:
3 shifting said binary representation of Q' to the left by 5 places to define a first shifted Q'
4 value,
5 shifting said binary representation of Q' to the left by 4 places to define a second shifted
6 Q' value; and
7 adding said first and second shifted values of Q' to the original value of Q'.

1 24. (Currently Amended) The system according to claim ~~[[14]]~~ 23, wherein said
2 multiplication of said second intermediate quotient (Q'') by 9 is accomplished by:
3 shifting said binary representation of Q' to the left by 5 places to define a first shifted Q'
4 value,
5 shifting said binary representation of Q' to the left by 4 places to define a second shifted
6 Q' value; and
7 adding said first and second shifted values of Q' to the original value of Q'.